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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/960,501	09/24/2001	Makoto Kakegawa	826.1753	7247

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EXAMINER	
LIN, SUN J	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 02/27/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/960,501	Applicant(s) KAKEGAWA, MAKOTO	
	Examiner Sun J Lin	Art Unit 2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-65* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-10,12-14,16-22,24-26,28-30,32-38,40-42,44-46,48-54,56-58,60-62,64 and 65* is/are rejected.

7)☒ Claim(s) *7,11,15,23,27,31,39,43,47,55,59 and 63* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 September 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This office action is in response to application 09/960,501 filed on 09/24/2001. Claims 1 – 65 remain pending in the application.

Claim Rejections - 35 USC § 102

2. The following is a quotation of 35 U.S.C. 102(b) which forms the basis for all obviousness rejections set forth in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 4, 6, 17, 20, 22, 33, 36, 38, 49, 52, 54 and 65 are rejected under 35 U.S.C. 102(b) as being unpatentable over U.S. Patent No. 5,375,069 to *Satoh et al.*

4. As to Claim 1, *Satoh et al.* show in Fig. 1 and teach the following subject matters:

- A *logic file 3* (i.e., logical circuit storage unit) for storing a logical circuit – [Fig. 1; col. 5, line 53 – 55];
- An *automatic wiring system 2* (i.e., transmission line circuit generation unit) for generating a *wiring route* (i.e., transmission line circuit) based on the logical circuit stored in the *logic file 3* (logical circuit storage unit) – [Fig. 1; col. 5, line 66 – col. 6, line 1]; and
- A *wiring result file 6* (i.e., transmission line circuit storage unit) for storing the *wiring route* (transmission lines circuit) generated by the *automatic wiring system 2* (transmission line circuit generation unit) – [Fig. 1].

For reference purposes, the explanations given above in response to Claim 1 are called **[Response A]** hereinafter.

5. As to Claims 17, 33 and 49, reasons are included in **[Response A]** given above. It is inherent that *logic file 3* is a storage of a *logical circuit database*; *wiring result file 6* is a storage of a *transmission line circuit database*.

6. As to Claim 65, reasons are included in **[Response A]** given above.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

(1). Determining the scope and contents of the prior art.
(2). Ascertaining the differences between the prior art and the claims at issue.
(3). Resolving the level of ordinary skill in the pertinent art.
(4). Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. Claim 2, 3, 8 – 10, 12 – 14, 16, 18, 19, 24 – 26, 28 – 30, 32, 34, 35, 40, 42, 44, 46, 48, 50, 51, 56, 58, 60, 62 and 64 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,046,017 to *Yuyama et al.* in view of U.S. Patent No. 5,375,069 to *Satoh et al.*

9. As to Claim 2, *Yuyama et al.* show in Fig. 3 and teach the following subject matters:

- Step S1 – *Design for Circuit of Cells*;
- Step S2 – *Design for Cells Layout*;
- Step S3 – *Drawing Rough Wiring*;
- Step S4 – *Estimate of Characteristic*;
- Step S5 – *Attain to Target Characteristic?* (i.e., Judgement Step);
- If result of *Judgment Step S5* is *negative* (i.e., "*NO*"), perform *redoing of design for cells (S1)*, *alternation of cells layout (S2)* ***or*** *alternation of rough wiring routes (S3)* – [col. 3, line 52 – 63].

Yuyama et al. teach that the *cell* may be a unit *circuit* such as *inverter*, *AND* or *OR* – [col. 2, line 42 – 43]. It is inherent that the *circuit of cell* is a *logical circuit*.

Yuyama et al. teach that the *rough wiring* is a *supposed wiring pattern* based on a *designated rough route* – [abstract; col. 2, line 4 – 6]. The *supposed shapes of wirings* (rough wiring) may not satisfy all of required *electrical and physical conditions*, including layout rules, in a semiconductor integrated circuit – [col. 3, line 14 – 17]. In other words, *the wiring routes among cells are only supposed before meeting target electrical and physical characteristic* – [col. 3, line 18 – 19]

It is inherent that the *supposed wiring pattern* is a *tentative transmission line circuit* of the *logical circuit* under study. *Alternation of rough wiring routes (S3)* is to *edit the transmission line circuit*. After the transmission line circuit is alternated/edited, if the result of *Judgement Step S5* is still "*NO*", *redoing of design for cells (S1)* is performed to *modify the logical circuit* – [col. 3, line 52 – 63].

It is inherent that the *Alternation of rough wiring routes (S3)* is performed by a *transmission line circuit editing unit* based on the old transmission line circuit stored in a storage unit (e.g., wiring result file). It is also inherent that the *redoing of design for cells (S1)* is performed by a *logical circuit modification unit* based on the transmission line circuit edited by the *transmission line circuit editing unit*.

Yuyama et al. do not teach a method of using a *logical circuit storage unit* and *transmission line storage unit* in designing a logical circuit. But *Satoh et al.* show in Fig. 1 and teach this method as explained in **[Response A]** given above. *Satoh et al.* teach utilizing a *logic file 3* (i.e., *logical circuit storage unit*) and a *wiring result file 6* (i.e., *transmission line storage unit*) in use of an *automatic wiring system* – [col. 5, line 66 – col. 6, line 2]. It is inherent that these two units are essential in efficiently managing storage and retrieval of data in processing of wiring routes in design a logical circuit.

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have used the teachings of *Satoh et al.* by using a *logic file 3* (*logical circuit storage unit*) and a *wiring result file 6* (*transmission line storage unit*) in an *automatic wiring system* in order to efficiently managing storage and retrieval of data in processing of wiring routes in design a logical circuit.

For reference purposes, the explanations given above in response to Claim 2 are called **[Response B]** hereinafter.

10. As to Claims 18, 34 and 50, reasons are included in **[Response B]** given above.

11. As to Claim 3, reasons are included in **[Response A]** and **[Response B]** given above.

For reference purposes, the explanations given above in response to Claim 3 are called **[Response C]** hereinafter.

12. As to Claims 19, 35 and 51, reasons are included in **[Response C]** given above.

13. As to Claims 4 and 8, *Satoh et al.* show in Fig. 1 and teach the following subject matters:

- A *logic diagram* (i.e., *topology designation table*) in *logic file 3* storing *topology information* indicating a *logical wiring data* (i.e., *type of connection*) between *gates* (i.e., active components) composing a logical circuit, and
- *Automatic wiring system 2* (i.e., *transmission line circuit generation unit*) generates a wiring route (transmission line circuit) based on the *logic wiring data* (topology information) stored in the *logic diagram* (*topology designation table*).

For reference purposes, the explanations given above in response to Claims 4 and 8 are called **[Response D]** hereinafter.

14. As to Claims 20, 24, 36, 40, 52 and 56, reasons are included in **[Response D]** given above.

15. As to Claims 28, 44 and 60 reasons are included in **[Response B]** given above.

16. As to Claims 32, 48 and 64, due to reasons given in **[Response B]** and according to Fig. 3 of *Yuyama et al.*, the following subject matters are inherent:

- Processing of S1 – S5 is a repeatable loop, which can be repeated many times dependent upon the result of *Judgment Step S5*;

- If result of *Judgment Step S5* is *negative* (i.e., "*NO*"), perform *redoing of design for cells (S1)*, *alternation of cells layout (S2)* **or** *alternation of rough wiring routes (S3)* – [col. 3, line 52 – 63];
- After *redoing S1*, the *logical circuit* (*circuit of cell*) is modified. It is inherent that the *modified logical circuit* is stored in a *logical circuit da*tabase for future verification;
- After the *wiring route* (*transmission line circuit*) is *alternated* (*edited*), if the result of S5 is "NO", Step S1 (*modified logical circuit*) may need to be repeated;
- ➔ Logical circuit is modified based on a difference between a wiring route by the editing and a logical circuit stored in the logical circuit database in the modifying.

For reference purposes, the explanations given above in response to Claims 32, 48 and 64 are called **[Response E]** hereinafter.

17. As to Claims 12 and 16, reasons are included in **[Response E]** given above. *Yuyama et al.*, teach that the logical circuit should satisfy all electrical and physical conditions. Therefore, the processing S1 – S5 is repeated many times in order to achieve this design goal.

18. Claims 5, 21, 37, 41, 45, 53, 57 and 61 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,375,069 to *Satoh et al.* in view of U.S. Patent No. 5,046,017 to *Yuyama et al.*

19. As to Claims 5, 21, 37, 41, 45, 53, 57 and 61, *Satoh et al.* show and teach all subject matters in Claim 1 including an *automatic wiring system* (*transmission line circuit generation unit*). *Satoh et al.* do not teach a method of storing a *value* of a *passive component* comprising a logical circuit in a *value designation table*, and generating a *transmission line circuit* based on the value stored in the *value designation table* using the *transmission line circuit generation unit* (*automatic wiring system*). But

Yuyama et al. teach that a *resistance value R* and *capacitance value C* in each wiring pattern are accurately determined based on *measured wiring length* and a *given resistance per unit length value* and a *given capacitance per unit length value* of the wiring pattern – [col. 3, line 29 – 34].

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have used the teachings of *Yuyama et al.* by using a *given resistance per unit length value* and a *given capacitance per unit length value* of a wiring pattern to accurately calculate the *total resistance value R* and *capacitance value C*, which are important factors in determining timing characteristic of the wiring pattern.

It is inherent that either *resistance* or *capacitance* is *passive component*. Since *resistance per unit length value* and *capacitance per unit length value* are given. Either one of values is stored in a *value designation table*.

For reference purposes, the explanations given above in response to Claims 5, 21, 37, 41, 45, 53, 57 and 61 are called **[Response F]** hereinafter.

20. As to Claim 9, *Yuyama et al.* teach that a *resistance value R* and *capacitance value C* in each wiring pattern are accurately determined based on *measured wiring length* and a *given resistance per unit length value* and a *given capacitance per unit length value* of the wiring pattern – [col. 3, line 29 – 34]. It is inherent that either *resistance* or *capacitance* is *passive component*. Since *resistance per unit length value* and *capacitance per unit length value* are given. Either one of values is stored in a *value designation table*.

21. As to Claims 13 and 29, reasons are included in **[Response E]** given above. It is inherent that, *after alternating/editing*, the length of the *wiring pattern* (*transmission line circuit*) is changed. The logical circuit is changed due to modification of previous resistance and capacitance value of the wiring pattern stored in the logical circuit storage unit.

22. As to Claim 21, reasons are included in **[Response F]** given above.

23. As to Claims 25, *Yuyama et al.* teach that a *resistance value R* and *capacitance value C* in each wiring pattern are accurately determined based on *measured wiring length* and a *given resistance per unit length value* and a *given capacitance per unit length value* of the wiring pattern – [col. 3, line 29 – 34]. It is inherent that either *resistance* or *capacitance* is *passive component*. Since *resistance per unit length value* and *capacitance per unit length value* are given. Either one of values is stored in a *value designation table*.

24. As to Claims 6, 10, 22, 26, 38, 42, 54 and 58, it is inherent that a inductor, which is a key unit of a *EMI filter*, is used to choke out *undesired AC signals* to/from a *logical circuit*, which is basically a *DC circuit unit*. To achieve this goal, it is inherent that *sufficient inductance* is required on each *transmission line* connecting to *input*, *output*, *power source* (V_{DD}) and *ground* (V_{SS}) of a logical circuit unit. Although part of inductance can be provided by the metal pattern of transmission line, it is usually not sufficient. Therefore, installing an *appropriate inductor unit* on the transmission line to compensate the deficiency is necessary. The *inductor unit* is a *passive component*. For easy retrieval, it is inherent that the (*inductance*) *addition information* of the *inductor unit* is stored in an *addition designation table*, which is a *database*, for use in designing transmission logical circuit by the transmission line circuit generation unit.

For reference purposes, the explanations given above in response to Claims 6, 10, 22, 26, 38, 42, 54 and 58 are called **[Response G]** hereinafter.

25. As to Claims 14, 30, 46 and 62 reasons are included in **[Response G]** given above. Notice that the *inductance addition information* included in the *addition designation table* may be inappropriate. Therefore, it is inherent that the *inductance addition information* should be modified to an appropriate value in order to meet real requirement.

Allowable Subject Matter

26. Claims 7, 11, 15, 23, 27, 31, 39, 43, 47, 55, 59 and 63 are objected to as being dependent upon a rejected base claim, but they would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Those claims are allowed is because that the prior art does not teach or suggest a logical circuit designing device comprising:

- An *deletion designation table* storing *deletion information* of a *passive component* composing a logic circuit, and wherein the *transmission line circuit generation unit* generates a transmission line circuit by *deleting the passive component* based on the *passive component deletion information* stored in the *deletion designation table*.

Conclusion

27. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sun J. Lin whose telephone number is (703) 308-4916. The examiner can normally be reached on Monday-Friday (9:00AM-6:00PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (703) 308-1323. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

Sun James Lin
Art Unit 2825
February 20, 2003

VUTHE SIEK
PRIMARY EXAMINER